Low-temperature formation of source-drain contacts in self-aligned amorphous oxide TFTs

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In future display backplanes the increased resolution requirements (4k2k) and frame-rate (120Hz) demands low parasitic capacitance and high speed switching thin-film transistors (TFTs). Amorphous oxide semiconductors (AOSs) TFTs with large gate-source/drain (S/D) overlap like in conventional etch-stop-layer (ESL) and back-channel-etch (BCE) configuration are less suitable. Self-Aligned (SA) device configuration is preferred. The S/D region conductivity enhancement is one of the major challenges in this configuration. Various integration techniques have been reported to enhance the conductivity of these S/D regions i.e. implant (B and P), UV illumination, metal-reduction (Ti and Al) and plasma treatments (Ar and H_2) [1-5]. In this study, we demonstrated high performance SA TFTs with amorphous-Indium-Gallium-Zinc-Oxide (a-IGZO) semiconductor whereby the S/D regions are reduced with Calcium (Ca) for conductivity enhancement [6]. Compared to Ti and Al, Ca is more reactive, rendering the a-IGZO conductive at lower temperatures. Moreover, the formed CaO can simply be removed by water, making device integration simpler. TFTs were made on glass substrate with a barrier layer on it [7]. In the first step a-IGZO is deposited and patterned and then the gate stack (200nm SiO_2 /100nm Mo) is formed. This is followed by Ca treatment as mentioned in Ref. 6. The reduction of exposed a-IGZO occurs during Ca annealing step. In the next step an interlayer stack of a barrier/200 nm PECVD SiO_2 was deposited. Post interlayer stack deposition, via and then S/D metal (100 nm Mo) were patterned, which followed by a final anneal. All process steps stayed below a thermal budget of 250°C. The TFTs show excellent electrical performance, with field-effect mobility of ~11.0 $cm^2/(V.s)$, sub-threshold slopes of 0.4 V/decade and off-currents < 1.0 pA and also nicely scale with channel spacing (SP) as shown in Fig. 1 below. We compared Ca treated a-IGZO sheet resistance to H_2 (Si_xN_y Interlayer) and Ar plasma treated a-IGZO sheet resistance and observed that Ca treated a-IGZO sheet resistance equals to 0.7 kΩ/□ compared to 0.8 kΩ/□ for H_2 plasma treated and 1.1 kΩ/□ for Ar plasma treated.

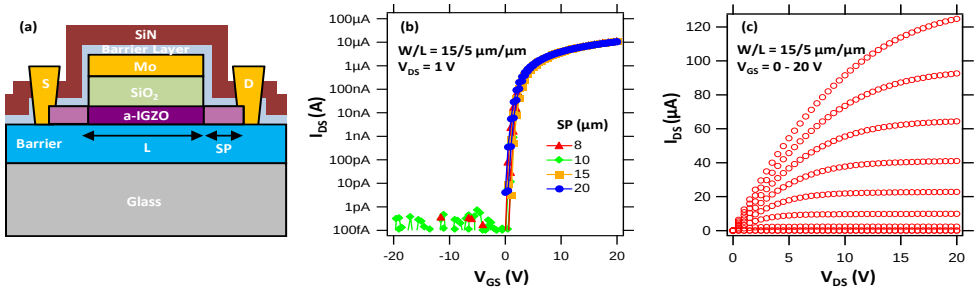

Fig 1. (a) Cross-sectional view, (b) transfer (V_{GS}/I_{DS}) characteristics dependence on spacing 'SP' scaling, (c) output (V_{DS}/I_{DS}) characteristics of SA TFTs.

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